AMENDMENTS TO THE SPECIFICATION:

Please replace the title with the following amended title:

DATA PROCESSOR SPEEDING UP REPEAT PROCESSING

Please replace the paragraph beginning at page 35, line 5, with the following amended paragraph:

In the E stage 403, the second operation unit [[116]] 117 performs all operations except addition of the multiply-add operation, such as arithmetic and logic operations, comparison, transfer and shift. Having received from the operand from the register file 115, the immediate value register 218 or accumulator 208 via the S$ bus 304, S5 bus 305, or some other dedicated path, each operation means of the second operation unit [[116]] 117 conducts the specified operation. The result of each operation is written back to the accumulator 218 or the register file 115 via the D2 bus 312 and the D3 bus 313.

Please replace the paragraph beginning at page 54, line 3, with the following amended paragraph:

As described above, the data processor according to Embodiment 1 possesses the hardware-implemented function that, independently of an operation specified by the instruction to be executed, detects the end of repeat processing in the repeat block, terminates the repeat processing prematurely halfway through the repeat block, and switches the instruction processing sequence to the next instruction in the repeat block. Accordingly, even when the number of repetitions of processing of the repeat block changes dynamically and the repeat processing

terminate prematurely halfway through the repeat block, the repeat block can be processed a predetermined number [[o]] of times at high speed using the same program. For example, in the case of repeating the multiply-add operation four times using the afore-mentioned EP instruction, too, if the data processor has no such hardware-implemented function of terminating the processing of the repeat block prematurely, synchronous execution of loading is allowed but it is necessary to decide which of at least four values 4n, 4n+1, 4n+2 and 4n+3 (where n is an integer equal to or greater than 1) the repeat count is. Of course, programs are necessary for the four repeat counts. Further, to deal with repeating the multiply-add operation three times or less, it is necessary to make a decision on the condition and prepare a program. In the case of preparing an operation library for the processing of the multiply-add operation or the like, too, the same problems arise if the repeat count is used as a parameter.

Please replace the paragraph beginning at page 55, line 19, with the following amended paragraph:

The data processor according to Embodiment 1 basically needs only to possess the hardware-implemented repeat function of processing a repeat block a predetermined number of times, and the function of terminating the repeat processing by the repeat processing terminating instruction halfway through the repeat block and switching the instruction processing sequence [[t]] to the next instruction in the repeat block. The data processor is not limited specifically to the configuration described above, and whatever hardware structure it has, the same results as described above could be obtained.

Please replace the paragraph beginning at page 80, line 19, with the following amended paragraph:

A variety of modifications may be ~~mad~~ made in Embodiment 6.